IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yeo, *et al.*	Docket No.:	TSM03-0511
Serial No.:	10/669,395	Art Unit:	2811
Filed:	September 24, 2003	Examiner:	Gebremariam, Samuel A.
Title:	Multiple-Gate Transistors Formed on Bulk Substrates		

Mail Stop: Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Affidavit filed under 37 C.F.R. § 1.132

Dear Sir:

I, Chao-Hsiung Wang, do hereby state that:

1. I am a Technical Manager working at Taiwan Semiconductor Manufacturing Co. Ltd in Hsin-Chu, Tawian.

2. I have a Ph.D. degree in Materials Science from the University of Cambridge, UK.

3. I have worked in the semiconductor industry for 7 years. During this time I have been an inventor on 8 patents and an author on 7 papers.

4. I have studied U.S. Patent No. 6,525,403 ('403 Patent) issued on February 24, 2003 to Satoshi Inaba and Kazuya Ohuchi.

5. I have reviewed and understand the structures illustrated in '403 Patent, including Figures 6 and 9. I see that these figures illustrate that source and drain regions 15 and 16 appear to have a junction that is spaced above the top surface of insulating film 12 and the bottom surface of gate electrode 14.

6. I have read and understand the specification of the '403 Patent. In particular, I have read and understand the portions of the specification that describe forming the illustrated structures.

7. Based upon what I have read in the specification, I would understand that the source and drain would extend at least to the top surface of insulating film 12 (and therefore the bottom surface of gate electrode 14) and would probably extend beneath the top surface of insulating film 12.

8. I understand from the paragraph beginning on line 34 of column 4 of the '403 Patent that the source diffusion layer 15 and drain diffusion layer 16 are formed after the gate electrode 14 was formed by introducing dopants into the side surfaces of the projection, except below the gate electrode, by means of ion implantation. I see that similar processes are disclosed in column 9, lines 5-12 and column 10, lines 23-38.

9. I am not aware of any doping process, including any ion implantation or vapor phase doping process, suitable for the structures shown and discussed in the '403 Patent that will create doped region in some but not all of an exposed surface.

10. Based upon what I have read in the specification of the '403 Patent, I would not know how to form a structure as shown in the figures of the '403 Patent that includes a source region or a drain region that has a source-substrate junction or a drain-substrate junction that is higher than the bottom surface of the gate electrode.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Date: 16 May 2005